REMARKS

The Examiner rejects claims 1 and 3-8 under 35 U.S.C. 102(e) as being anticipated by Dorsey et al ("Dorsey"), and claims 2 and 4-13 under 35 U.S.C. 103(a) as being unpatentable over Dorsey. Applicant continues respectfully to traverse these nonobvious conclusions by the Examiner.

Dorsey receives packet data units (PDUs) from a network interface 20a for storage in an input memory 21a. The packet headers and trailers from the input memory are input to a multi-protocol translator (MPT) 26 for translating into new headers and trailers which are stored in new PDUs in an output memory 21b. The data from the PDUs are transferred by direct memory access (DMA) 27 to the new PDUs in the output memory, or alternatively transferred via the MPT where the trailer needs to be formulated based upon the contents of the entire patent, i.e, error detection/correction fields. In other words, Dorsey does not analyze the data content of the PDUs as that is merely transferred from the input memory to the output memory, and merely translates the headers and trailers from the input memory from one protocol to another for output to the output memory.

The MPT receives a packet at the input memory and, according to the protocol of the packet and the protocol of the destination, loads information into the information FIFOs 54, 55 accordingly. Based upon the translation required the appropriate set of opcodes are selected from the opcode memory 51a. In operation the packet data is passed through from the input memory to the output memory and portions of the packet header/trailer are dumped, substituted for from the FIFO or passed through in sequence from the input memory to the output memory to

translate the input header/trailer to the output header/trailer. Contrary to the Examiner's conclusion, this translation process does not involve analysis of the protocol data except to the extent necessary to determine which set of opcodes are required for the translation (based upon source and destination addresses).

The Examiner equates the input memory 21a of Dorsey to Applicant's claimed data memory; the opcode memory 51a to Applicant's claimed microcode memory; the input memory 53a of the MPT to Applicant's claimed data register; [not clear -- opcode memory cannot be both memory and register] to Applicant's microcode register; the output memory of the MPT 58 (or output memory 21b?) to Applicant's output memory; the address control 53b to Applicant's claimed first addressing unit; and the address control 51b to Applicant's second addressing unit. The Examiner makes several mistakes in the above analysis, as is discussed below:

(a) The first addressing unit addresses the "data memory" according to claim 1, yet according to the Examiner the first addressing unit addresses the "data register" 51a and not the "data memory" 21a. In fact the input memory of the MPT of Dorsey is more akin to the data memory of Applicant, which means there is no data register corresponding to that claimed by Applicant.

(b) The claimed microcode memory stores "a microcode that represents at least a part of the communication protocol", whereas the opcode memory of Dorsey stores sets of translation instructions with one of them being selected according to the translation required by adjusting the start address in the opcode address control 51b. Each set is a complete set of instructions required for a particular translation.

(c) The claimed data register is "for reading out a pre-determined number of bits from the data memory", whereas Dorsey reads out bytes from the input memory

53a and either "dumps" them (by transferring them to a dump memory or by skipping the address from the address control 53b) or transfers them to the output memory – there is no data register separate from the input/data memory.

(d) Likewise there is no microcode register in Dorsey "for reading out a pre-determined number of bits from the microcode memory, with the content of the microcode register being usable for analyzing the content of the data register", as Dorsey uses the instructions from the selected set of instructions in the opcode memory to (i) readout bytes from the input memory to the output memory, (ii) readout bytes from the FIFO to the output memory or (iii) transfer operands from the opcode memory to the output memory – none of these are usable for analyzing the content of the data.

(e) Finally the address control units of Dorsey are not "designed to take into account the content of the data register and/or the microcode register when subsequent addresses are determined" as is recited by Applicant since Dorsey does not in fact have such registers. The statements by the Examiner related to writing into the output memory are irrelevant to this element in Applicant's claim since these claims deal with addressing the data and microcode memories, not the output memory.

With regards to claim 3 the Examiner *now* equates the claimed data register with the storage alignment units 93a of Dorsey, which units serve to hold data to be written to the output memory in later clock cycles, i.e., if a byte is available on one of channel A or B before corresponding data on the other channel, then the byte may be held for one or more clock cycles so corresponding bytes from the two channels may be written into the output memory at the same time. There is no indication of

shifting content, just aligning with another channel.

With respect to claim 4 the Examiner equates the output memory address control of Dorsey to the register block claimed by Applicant. The Examiner then talks about the addressing of the output memory. However claim 4 recites that the register block, which has "at least one register and at least one counter", contains contents "which are taken into account for determining the subsequent addresses for the first and second addressing units", i.e., addresses for the data memory and the microcode memory. This has nothing to do with the output memory.

Claim 5 recites that the address in the third processing unit, which does address the output memory, is "changeable by taking the content of the microcode register into account." Dorsey does not show an output from the opcode memory (since there is no microcode register in Dorsey – see above) that changes the address of the output memory address control.

Claim 6 recites that an entry from "the output memory is read out, changed to take into account a new result, and rewritten into the output memory." This is essentially a read/modify/write operation that is not shown or suggested by Dorsey nor is it required for protocol translation.

Claim 8 recites that the entry in the output memory is a parameter identifier and value -- analyzed data, whereas Dorsey teaches that the entry in the output memory is a data packet translated from one protocol to another.

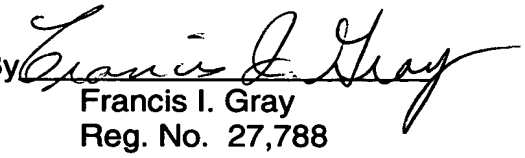
For the reasons discussed above, claims 10-13 also are deemed to be allowable.

Thus claims 1-13 are deemed to be allowable as being neither anticipated nor rendered obvious to one of ordinary skill in the art by Dorsey.

In view of the foregoing remarks allowance of claims 1-13 is urged, and such action and the issuance of this case are requested.

Respectfully submitted,

BIRGER GERNHARDT

By 
Francis I. Gray
Reg. No. 27,788
Patent Agent for Applicant

TEKTRONIX, INC.
P.O. Box 500 (50-LAW)
Beaverton, OR 97077
(503) 627-7261

7031 US